IN THE SPECIFICATION

Please replace the paragraph beginning on page 2, line 2 with the following rewritten paragraph:

Conversely, data to be sent by the second user terminal 46 is sent to the modem interface 34 of the RNT 40. The data is processed to be in a format suitable for the transmit circuitry ~~32~~ 36 of the modem 28. The transmit circuitry 36 converts the processed data into a format suitable for transfer over the air interface 38. The data is subsequently transmitted over the air interface 38 using an antenna 42 and received by the base station 30. The received data is processed by the receive circuitry ~~34~~ 32 of the base station's modem 28. The processed data is further processed by the modem interface 34 to be in a format suitable for transmission through the RDU 24 and local exchange 22. The data is subsequently transferred through the RDU 24 and local exchange 22 to the user terminal 20.

Please replace the paragraph beginning on page 2, line 17 with the following rewritten paragraph:

A modem interface transfers data between the high data rate interface and a wireless interface. The ~~wireless~~ modem interface has a plurality of parallel data highways. Each data highway has frames with time slots for transferring data. The plurality of highways outputs data to the high data rate interface and the wireless

interface in selected time slots. At least one of the data highways has an input configured to receive data from the high data rate interface in selected time slots. At least one of the data highways has an input configured to receive data from the wireless interface in selected time slots. A processor controls the transfer of data between the plurality of highways.

Please replace the paragraph beginning on page 3, line 7 with the following rewritten paragraph:

Figure 2 illustrates a modem interface 56. As shown in Figure 3, the modem interface 56 is used to transfer data between a high data rate terminal, such as an integrated services digital network (ISDN) terminal 60, and a wireless air interface 38. Elements shown in Figure 3 that correspond to elements shown in Figure 1 have been given like reference numerals. A modem 48 includes the modem interface 56, receive circuitry 52, and transmit circuitry 54. The modem interface 56 may be located on the RNT side of the wireless air interface as being a component of the RNT 40. Similarly the modem interface 56 may be used on the base station side of the air interface ~~56~~ 38, such as within the RCS 26. The modem interface 56 is preferably located at both the RNT 40 and RCS 26.

Please replace the paragraph beginning on page 3, line 14 with the following rewritten paragraph:

If used on the RNT side, the modem interface 56 receives data from the ISDN terminal 60 over an ISDN oriented modular-2 highway (IOM-2 highway) 62 (shown as reference numeral 44 in Figure 3), preferably at an E1 data rate. Conversely, the modem interface 56 also sends data to the ISDN terminal 60 over the IOM-2 highway 62. If used on the base station side, the modem interface 56 transfers data to and from the RDU 24 over a pulse code modulation (PCM) highway 62 (shown as reference numeral 58 in Figure 3), preferably at an E1 data rate.

Please replace the paragraph beginning on page 5, line 22 with the following rewritten paragraph:

PCM highway II 68_2 is used to transfer data to and from the digital signal processor (DSP) 78 using TS0-TS7. One such DSP 78 is a 54x family processor, preferably a TMS320C54x processor. The DSP 78 may perform functions such as speech, video compression or encryption. Data is read from the PCM highway II 68_2 using a group of read devices 80_1-80_n. The read data is buffered by a group of buffers 84_1-84_n and then sent to the DSP 78. Data sent from the DSP 78 is buffered by a group of buffers 86_1-86_n and then written into the corresponding time slots of

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the PCM highway II 68_2 using a group of write devices 82_1-82_n. TS8 - TS15 of the PCM highway II 68_2 are used to interface with telephone interface components.

Please replace the paragraph beginning on page 6, line 20 with the following rewritten paragraph:

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TS0-TS8 of PCM highway III 68_3 are used for HDLC processing. Data in TS0-TS8 are read by the HDLC reading devices 108_1-108_{n3}. Data from TS0 - TS2 is processed by an HDLC multiplexer (HMUX) 112 which sends processed data to an input/output (I/O) device 116 and an HDLC I controller 114_1. Data is also sent from the I/O devices 116 and HDLC I controller 114_1 to the HMUX 112. The data processed by the HMUX 112 from the I/O device 116 and HDLC I device 114_1 is written to TS0-TS2 of PCM highway III 68_3 using a HDLC write device 110_1. Data in TS3-TS8 is transferred to and from the other two HDLC controllers (HDLC II ~~110_2~~ 114_2, TS3-TS5, and HDLC III ~~110_3~~ 114_3, TS6-TS8). The data in the corresponding slots is read by HDLC read devices 108_2, 108_3 prior to being sent to the corresponding HDLC controller 114_2, 114_3. Data from the HDLC II 114_2 and HDLC III 114_3 controllers is sent to the HDLC write devices 110_2, 110_3 and written onto the corresponding slots of PCM highway III 68_3. Data from each of the three HDLC controllers (HDLC I 114_1, HDLC II 114_2 and HDLC III 114_3) is transferred

back and forth to the ARM processor 88. The HDLC controllers 114_1-114_3 are used to communicate~~d~~ with the ARM processor 88 or the traffic channels.

Please replace the paragraph beginning on page 7, line 19 with the following rewritten paragraph:

Conversely, the HDLC controllers 114_1-114_3 also decode a double HDLC encoded D channel received over the wireless interface 38. The double HDLC encoded D channel is stripped of the second HDLC encoding by the HDLC controllers 114_1-114_3. The CRC field data is used to correct any errors that occurred during the wireless transfer. Accordingly, the original D channel is recovered. Preferably, each HDLC controller 114_1-114_3 processes data at 384 Kbs and ~~require 3~~ requires three 128 Kbs time slots.

Please replace the paragraph beginning on page 7, line 25 with the following rewritten paragraph:

TS9-11 of PCM highway III 68_3 are used to transfer data to and from the ARM processor 88. A group of read devices 100_1-100_n read data from the corresponding slots of PCM highway III 68_3. The read data is buffered by a group of buffers 102_1-102_n and is sent to the ARM processor 88. The ARM processor 88 sends

data to a group of buffers ~~94_1-94_n~~ 104_1-104_n. The buffered data is written by corresponding write devices 106_1-106_n onto PCM highway III 68_3.

Please replace the paragraph beginning on page 8, line 21 with the following rewritten paragraph:

Data to be sent over the wireless interface 38 is read by a group of read devices 118_1-118_4. One read device 118_1-118_4 is used per traffic channel, TR0-TR3. Another set of read devices 120_1-120_4 is used for encryption of each ~~channels~~ channel's data ~~120_1-120_4~~. The output of ~~one 120_1-120_4 of~~ each channel's encryption read devices 120_1-120_4 is input into a parallel to serial converter ~~122_1-122_4~~ 124_1-124_4. The serial output of that converter 124_1-124_4 is fed into another parallel to serial converter ~~124_1-124_4~~ 122_1-122_4 which also receives the output of the other one of that channel's read devices 118_1-118_4. The two serial outputs are modulo-2 added on a bit basis to encrypt the data. Each channel's encrypted serial output is typically sent to a corresponding convolutional encoder, spreader and modulator for transfer over the wireless interface 38. Each parallel to serial converter 118_1-118_4 is programmed to produce data at a desired bit rate.

Please replace the paragraph beginning on page 9, line 7 with the following rewritten paragraph:

Encrypted data received from traffic channels, such as QVD_TR0-QVD_TR3, is input to a group of serial to parallel converters 126_1-126_4. Each channel's serial to parallel converter 126_1-126_4 combines that traffic channel's data with an output of a parallel to serial converter 128_1-128_4 to decrypt the traffic data. The decryption data from each parallel to serial converter 128_1-128_4 originates from data read from TS12-TS15 by corresponding read devices 138_1-138_4. The read data is converted from parallel to serial format by the parallel to serial converters 128_1-128_4. The serial outputs of the serial to parallel converters 126_1-126_4 are inputted to a group of write devices 132_1-132_4 which write the serial output to a group of multiplexers 130_1-130_4. The multiplexed data is sent to TS12-TS15 of the PCM highway III 68_3. For testing, the DSP 78 outputs a signal to a group of buffers 136_1-136_4. The output of the buffers 136_1-136_4 is also input to the multiplexers 130_1-130_4 through a corresponding group of write devices 134_1-134_n.

Please replace the Abstract with the following rewritten paragraph:

A modem interface transfers data between ~~the~~ a high data rate interface and a wireless interface. The ~~wireless~~ modem interface has a plurality of parallel data highways. Each data highway has frames with time slots for transferring data. The plurality of highways outputs data to the high data rate interface and the wireless interface in selected time slots. At least one of the data highways has an input

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configured to receive data from the high data rate interface in selected time slots. At least one of the data highways has an input configured to receive data from the wireless interface in selected time slots. A processor controls the transfer of data between the plurality of highways.